**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A method of adding a first floating point number to a second floating point number, wherein the first floating point number is associated with a first mantissa, and the second floating point number is associated with a second mantissa, the method comprising:

adding the first mantissa, second mantissa, and an input bit together to produce a third mantissa and an output bit;

generating the input bit based on the first mantissa, second mantissa, and output bit; and

~~adding a first mantissa, a second mantissa, and an input bit together to produce a third mantissa;~~

normalizing the third mantissa to produce a final mantissa, wherein the third mantissa and the final mantissa are correctly rounded as a result of the act of adding.

2. (Currently Amended) The method according to claim 1, wherein generating the input is further based on a plurality of carry logic signals based on the second mantissa ~~the act of adding produces an output bit and wherein the input bit is derived from the output bit to ensure that the third mantissa is correctly rounded~~.

3. (Original) The method according to claim 1, wherein a less significant bit of the third mantissa depends on a more significant bit of the first mantissa.

4. (Original) The method according to claim 1, further comprising:
prior to the act of adding, aligning the first mantissa with the second mantissa.

5. (Original) The method according to claim 1, further comprising:

prior to the act of adding, if both of the two floating point numbers are positive, shifting a larger or equal floating point number of the two floating point numbers by one position to produce the first mantissa.

6. (Original) The method according to claim 1, further comprising:

prior to the act of adding, if both of the two floating point numbers are positive, shifting

in a number of zeroes into a smaller or equal floating point number of the two floating point numbers to produce a series of control variables and a fourth mantissa having digits; and

complementing each digit of the fourth mantissa to produce the second mantissa.

7. (Currently Amended) A method of adding a first floating point number to a second floating point number, the method comprising:

unpacking the first floating point number, having a first exponent and a first mantissa of X bits, to generate a second mantissa of at least X+K bits, wherein X and K are positive integers;

unpacking the second floating point number having a third mantissa of X bits to generate a fourth mantissa of at least X+K bits;

adding the second~~a first~~ mantissa to the fourth~~a second~~ mantissa to produce a fifth mantissa of X+K bits; and

~~adding a fourth mantissa to an input bit to round the fourth mantissa;~~

normalizing the fifth~~a third~~ mantissa~~;~~

~~wherein the acts of adding are integrated together within a single adder to produce the third mantissa~~.

8. (Currently Amended) The method according to claim 7, wherein when the first exponent is 0, bits 00 are supplemented to the first mantissa, otherwise bits 01 are supplemented to the first mantissa ~~a less significant bit of the third mantissa depends on a more significant bit of the first mantissa~~.

9. (Currently Amended) A method of adding a first floating point number to a second floating point number, the method comprising:

adding a first mantissa, associated with the first floating point number, a second mantissa, associated with the second floating point number, and an input bit together to produce a third mantissa and an output bit;

rounding the third mantissa by updating the input bit based on the output bit to produce a fourth mantissa;

normalizing the fourth mantissa; and

integrating the acts of adding and rounding within a single adder so that a separate adder to produce a correctly rounded result is not needed and so that the acts of adding and rounding are performed prior to the act of normalizing.

10. (Original) The method according to claim 9, wherein a less significant bit of the fourth mantissa depends on a more significant bit of the fourth mantissa.

11. (Currently Amended) A method of adding a first floating point number to a second floating point number, the method comprising:

receiving a first floating point number having a first mantissa and a second floating point number having a second mantissa~~, the first floating point number when added to the second floating point number producing a third floating point number having a third mantissa~~;

respectively ~~left~~-shifting the first mantissa and the second mantissa as appropriate to obtain a fourth mantissa and a fifth mantissa;

producing a first carry bit from a second carry bit and from round control variables derived from the first mantissa and the second mantissa;

adding the fourth mantissa, the fifth mantissa and the first carry bit together to produce a sixth mantissa and the second carry bit, wherein the sixth mantissa is correctly rounded; and

~~right~~-shifting the sixth mantissa to produce the third mantissa.

12. (Original) The method according to claim 11, wherein a less significant bit of the sixth mantissa depends on a more significant bit of the fourth mantissa.

13. (Currently Amended) A floating point adder system to add a first floating point number to a second floating point number, the system comprising:

an adder to perform an add operation to add a first mantissa, associated with the first floating point number, a second mantissa, associated with the second floating point number, and an input bit together to produce a third mantissa and an output bit;

a carry logic circuit coupled to the input bit and generating the output bit; and

a shifter coupled to the adder to normalize the third mantissa to produce a final mantissa,

wherein the third mantissa and the final mantissa are correctly rounded as a result of the add operation performed by the adder.

14. (Currently Amended) The system according to claim 13, wherein the carry logic circuit comprises an OR gate and an AND gate~~further comprising:~~

~~round control logic coupled to the adder to provide the input bit to the adder and to derive the input bit from an output bit produced by the adder during the add operation to ensure that the third mantissa is correctly rounded~~.

15. (Original) The system according to claim 13, wherein a less significant bit of the third mantissa depends on a more significant bit of first mantissa.

16. (Currently Amended) A computer readable medium containing programming instructions for adding a first floating point number to a second floating point number, said programming instructions comprising instructions for:

adding a first mantissa, associated with the first floating point number, a second mantissa, associated with the second floating point number, and an input bit together to produce a third mantissa and an output bit;

generating the input bit using the output bit; and

normalizing the third mantissa to produce a final mantissa, wherein the third mantissa and the final mantissa are correctly rounded as a result of the act of adding.

17. (Currently Amended) A floating point adder system to add a first floating point number to a second floating point number, the system comprising:

means for adding a first mantissa, associated with the first floating point number, a second mantissa, associated with the second floating point number, and an input bit together to produce a third mantissa and an output bit;

means for ~~rounding the third mantissa by~~ updating the input bit based on the output bit ~~to produce a fourth mantissa~~;

means for normalizing the third~~fourth~~ mantissa~~, wherein the means for adding and the means for rounding are integrated together within a single adder coupled to round control logic so that a separate adder to produce a correctly rounded result is not needed~~.